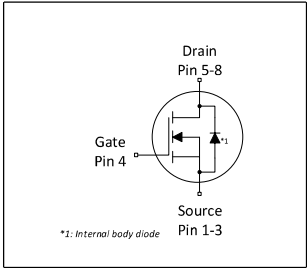
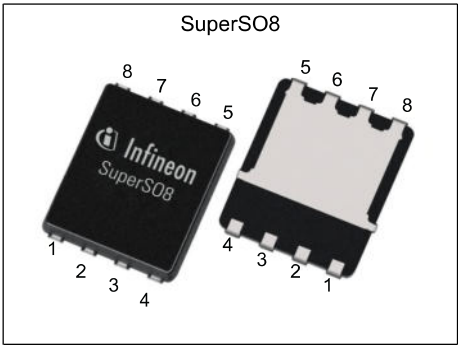


MOSFET

OptiMOS™ 3 Power-Transistor, 75 V

Features

- Optimized technology for synchronous rectification
- Ideal for high frequency switching and DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Halogen-free according to IEC61249-2-21



RoHS

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	75	V
$R_{DS(on),max}$	4.2	mΩ
I_D	132	A

Type / Ordering Code	Package	Marking	Related Links
BSC042NE7NS3 G	PG-TDSON-8	042NE7NS	-

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	132 83 19	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	528	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	220	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	125 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{2)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.0	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	18	K/W	-
Device on PCB, minimal footprint	R_{thJA}	-	-	62	K/W	-
Device on PCB, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	50	K/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	75	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.3	3.1	3.8	V	$V_{DS}=V_{GS}$, $I_D=91\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1.0 100	μA	$V_{DS}=75\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=75\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.7	4.2	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$
Gate resistance	R_G	-	2.2	-	Ω	-
Transconductance	g_{fs}	44	89	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	3600	4800	pF	$V_{GS}=0\text{ V}$, $V_{DS}=37.5\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	810	1100	pF	$V_{GS}=0\text{ V}$, $V_{DS}=37.5\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	40	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=37.5\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=37.5\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_G=1.8\text{ }\Omega$
Rise time	t_r	-	17	-	ns	$V_{DD}=37.5\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_G=1.8\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	34	-	ns	$V_{DD}=37.5\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_G=1.8\text{ }\Omega$
Fall time	t_f	-	9	-	ns	$V_{DD}=37.5\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_G=1.8\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	18.3	-	nC	$V_{DD}=37.5\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	10.4	-	nC	$V_{DD}=37.5\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	17.6	-	nC	$V_{DD}=37.5\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	52	69	nC	$V_{DD}=37.5\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.1	-	V	$V_{DD}=37.5\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	53	71	nC	$V_{DD}=37.5\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	90	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	528	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.89	1.2	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	44	-	ns	$V_R=40\text{ V}$, $I_F=25\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	64	-	nC	$V_R=40\text{ V}$, $I_F=25\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

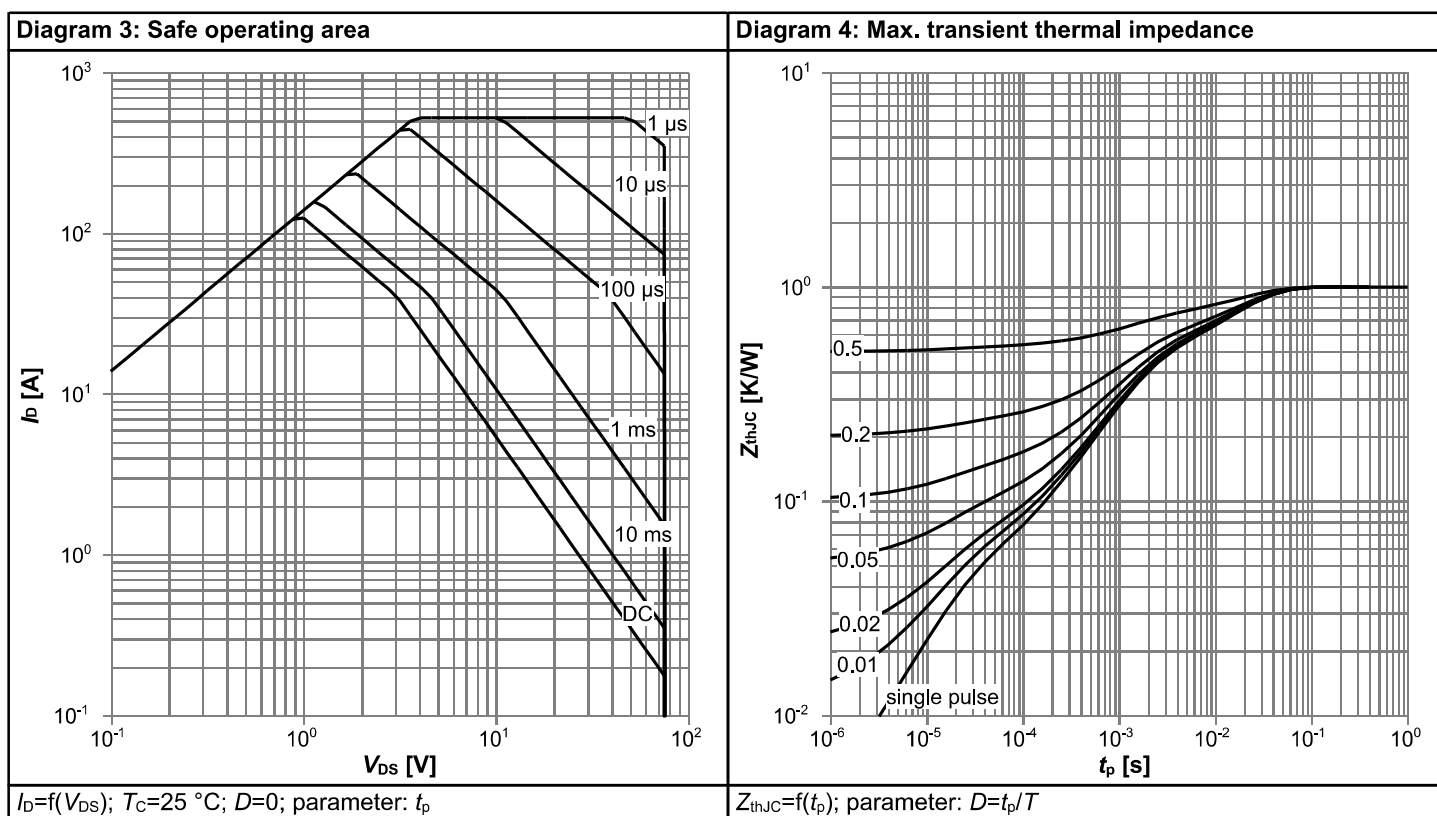
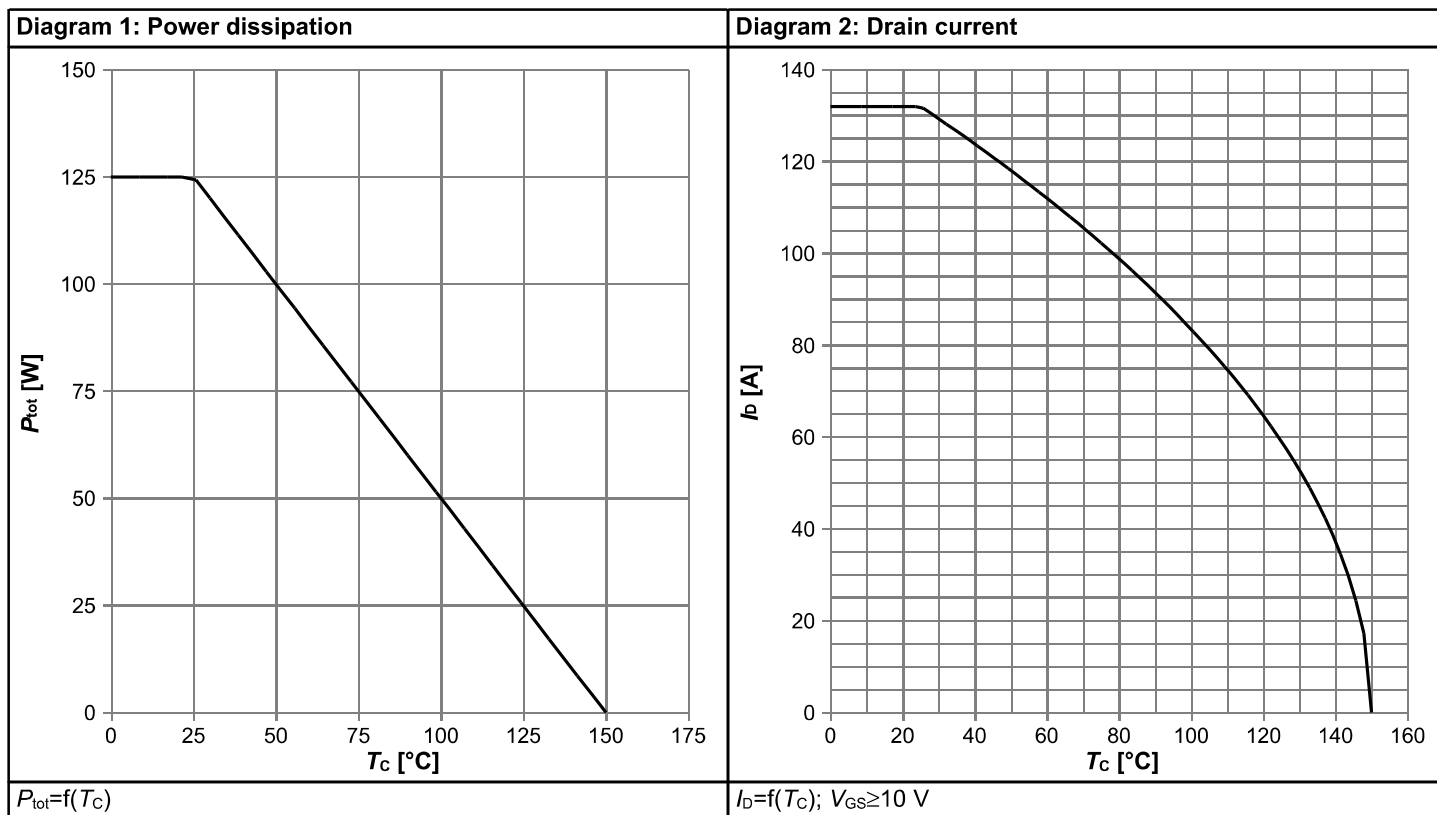
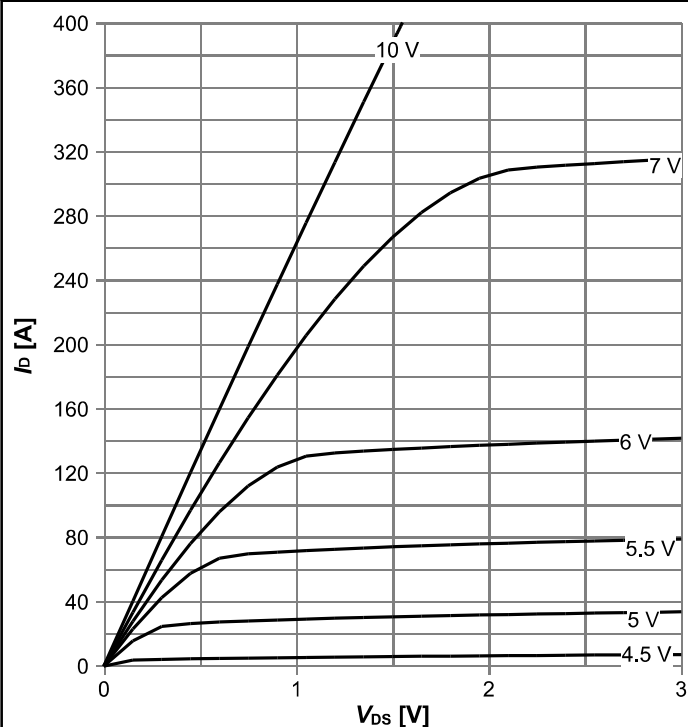
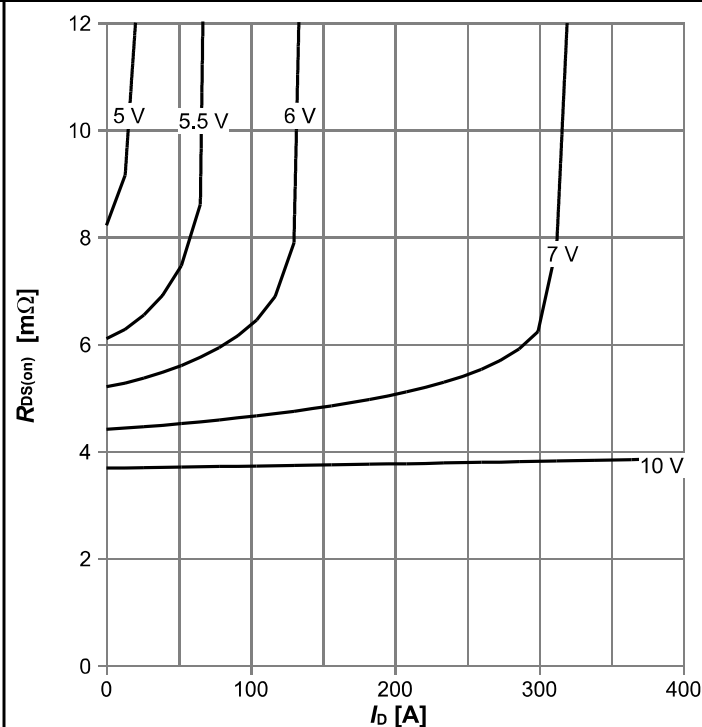


Diagram 5: Typ. output characteristics



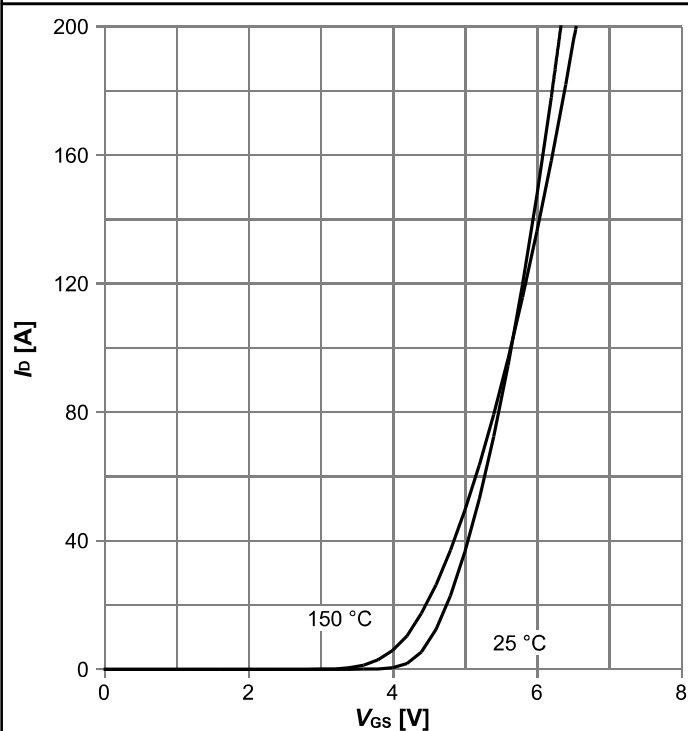
$I_D = f(V_{DS})$; $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



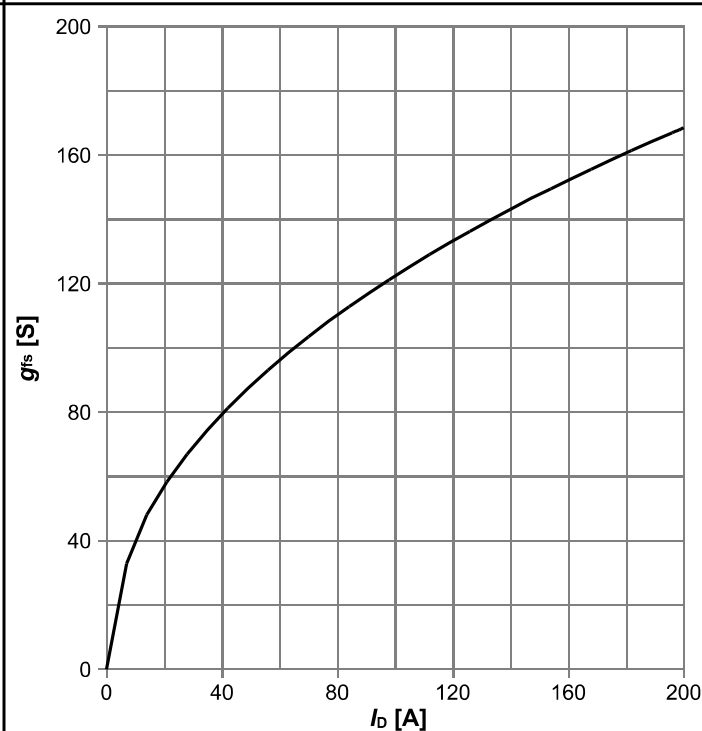
$R_{DS(on)} = f(I_D)$; $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



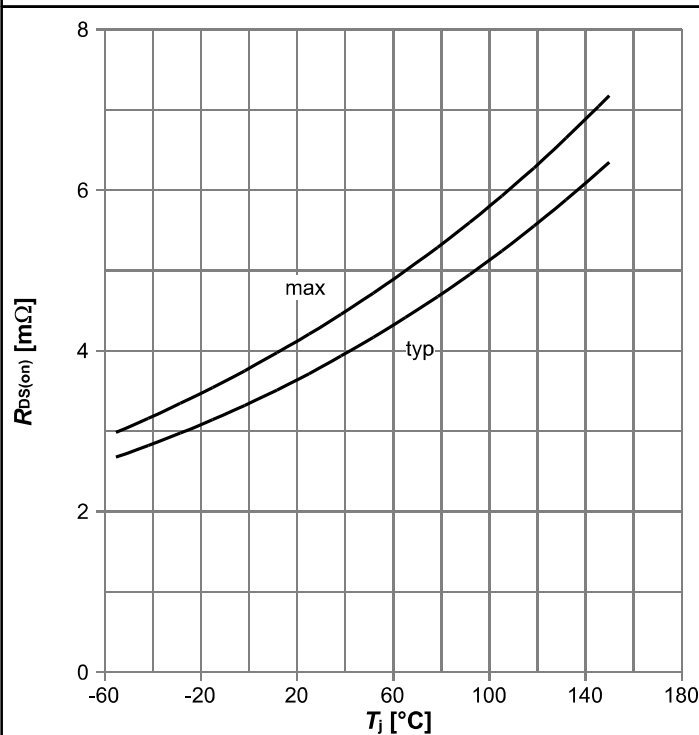
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_J

Diagram 8: Typ. forward transconductance



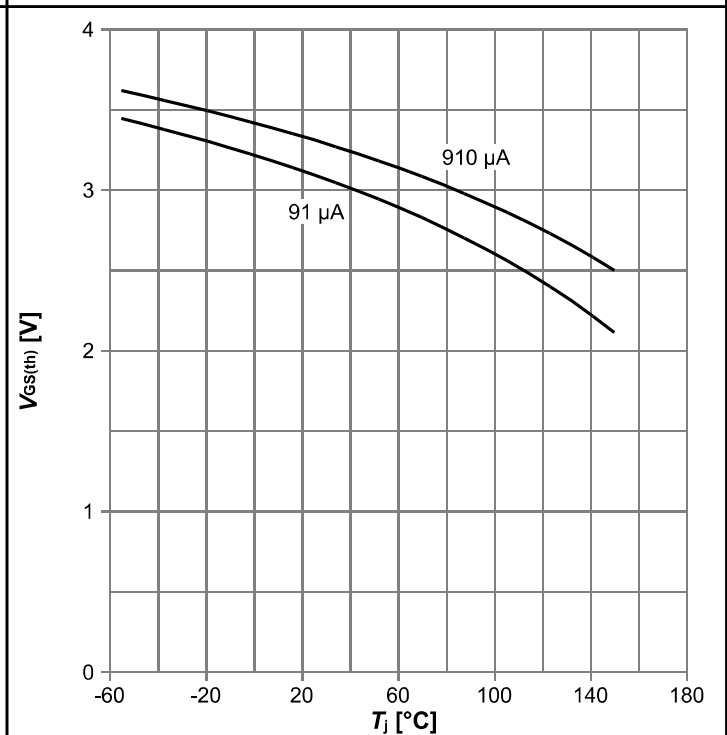
$g_{fs} = f(I_D)$; $T_J = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



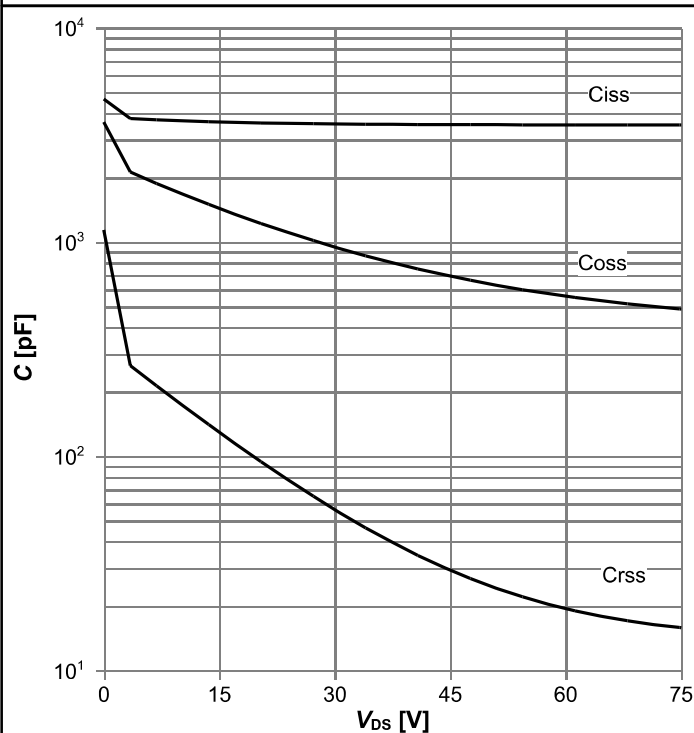
$R_{DS(on)}=f(T_j)$; $I_D=50$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



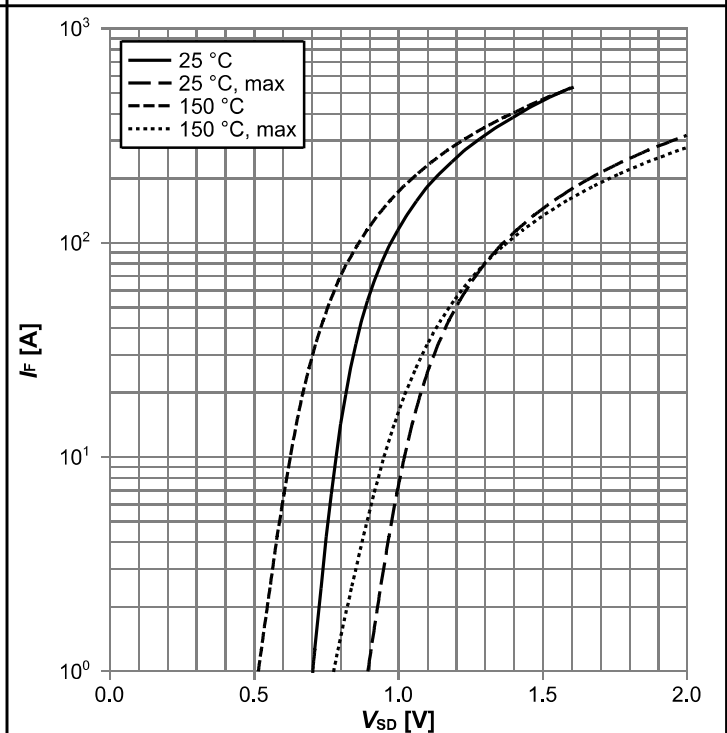
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode

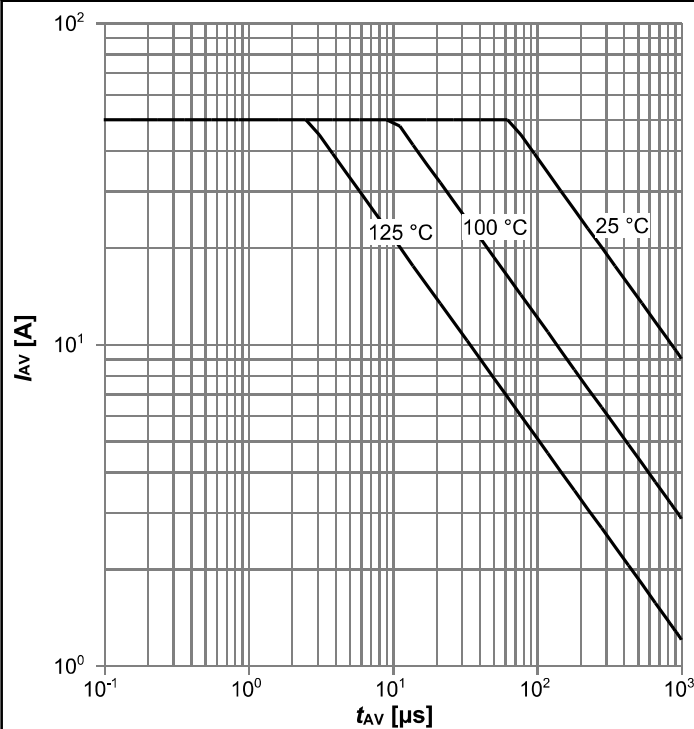


$I_F=f(V_{SD})$; parameter: T_j

OptiMOS™ 3 Power-Transistor, 75 V

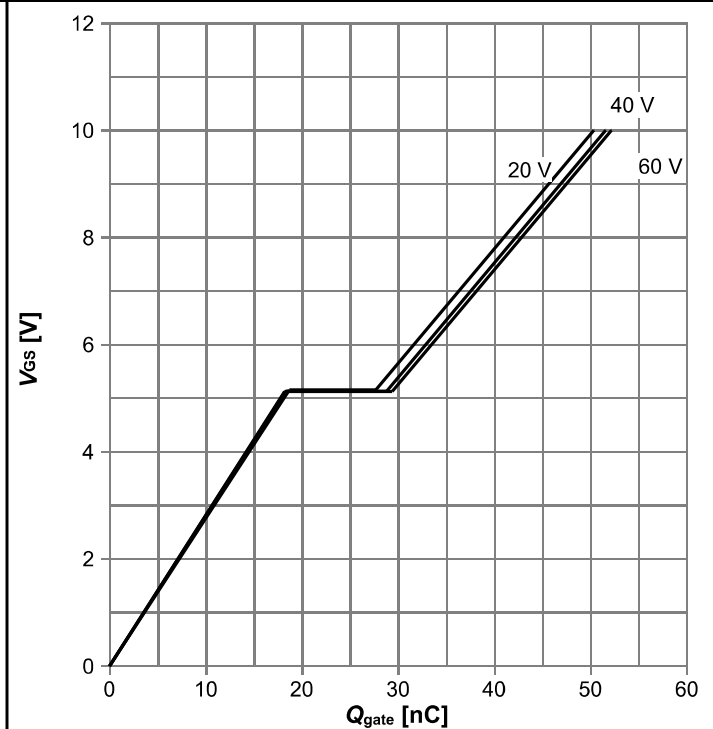
BSC042NE7NS3 G

Diagram 13: Avalanche characteristics



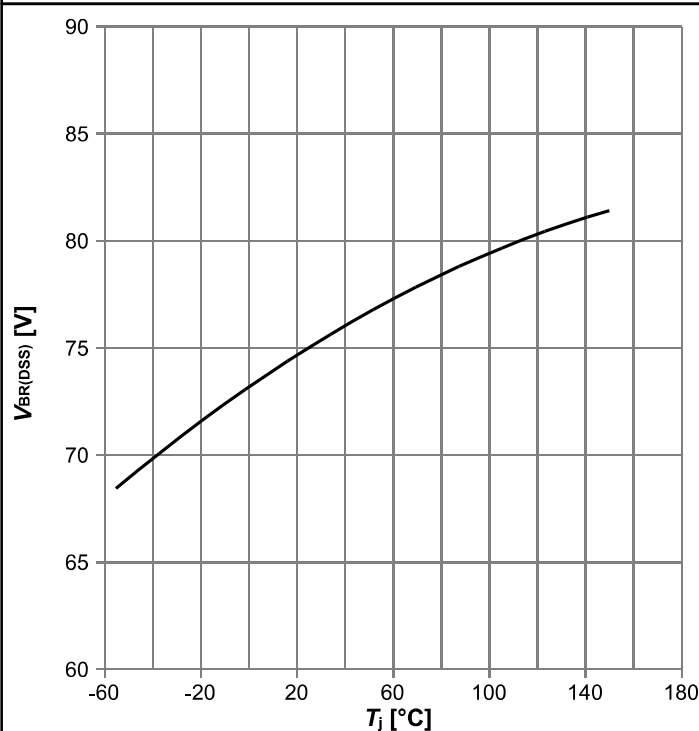
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



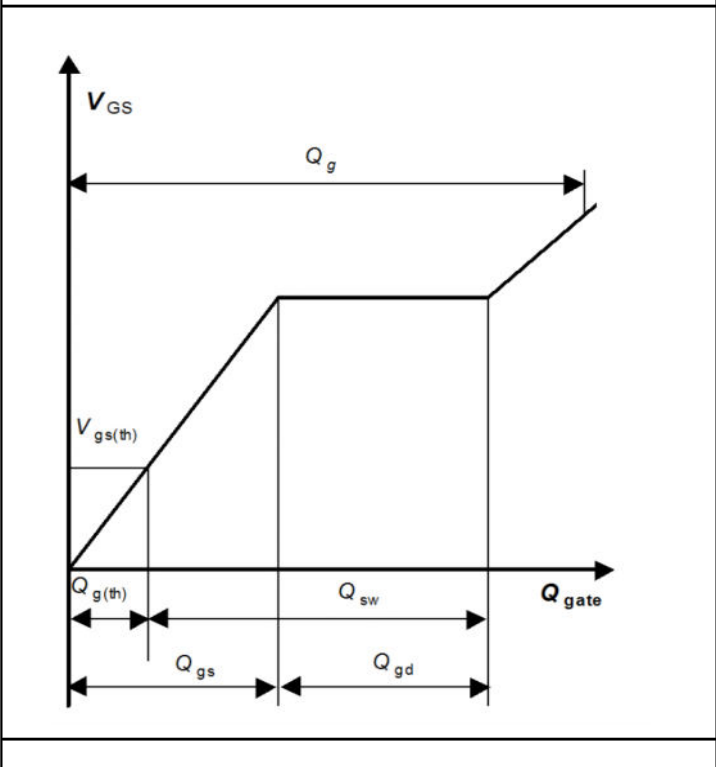
$V_{GS}=f(Q_{gate})$; $I_D=50\text{ A}$ pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

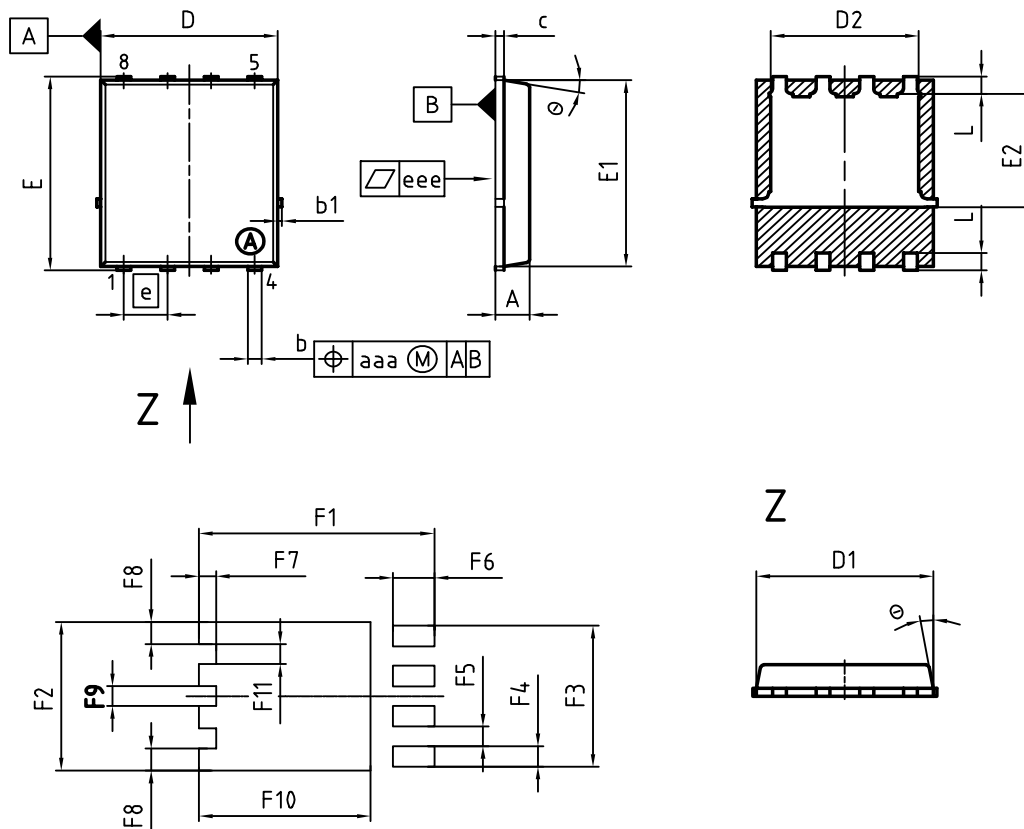


$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.02	0.22	0.001	0.008
c	0.15	0.35	0.006	0.014
D=D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	3.40	3.80	0.134	0.150
e	1.27		0.050	
N	8		8	
L	0.45	0.65	0.018	0.026
θ	8.5°	11.5°	8.5°	11.5°
aaa	0.25		0.010	
eee	0.05		0.002	
F1	6.75	6.95	0.266	0.274
F2	4.60	4.80	0.181	0.189
F3	4.36	4.56	0.172	0.180
F4	0.55	0.75	0.022	0.030
F5	0.52	0.72	0.020	0.028
F6	1.10	1.30	0.043	0.051
F7	0.40	0.60	0.016	0.024
F8	0.60	0.80	0.024	0.031
F9	0.53	0.73	0.021	0.029
F10	4.90	5.10	0.193	0.201
F11	0.53	0.73	0.021	0.029

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REVISION 03

Figure 1 Outline PG-TDSON-8, dimensions in mm/inches

Revision History

BSC042NE7NS3 G

Revision: 2021-05-10, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2021-05-10	Update current rating and footnotes

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